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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,481	12/10/2003	Ui Sik Kim	P69373US0	5399

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,481	KIM, UI SIK	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 9-19 is/are allowed.

6)☒ Claim(s) 1,3 and 8 is/are rejected.

7)☒ Claim(s) 2 and 4-7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Application filed 12/10/2003.

Currently, claims 1-19 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

112 Issues have been resolved.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (U.S. Patent No. 6,815,275 filed 9/27/2002) in view of Dass et al. (U.S. Patent No. 5,536,684 dated 7/16/1996) and Mikagi (U.S. Patent No. 6,284,662 dated 9/4/2001).

Kwon shows the method substantially as claimed in Figs. 3A-5 and corresponding text as: forming a gate (109) on a predetermined area of a semiconductor substrate (100) (col. 3, line 56-col. 4, line 8), forming spacers (110a, 112a) on sidewalls thereof (col. 4, lines 9-29), and then forming a junction area (114) in a predetermined area of the semiconductor substrate (col. 4, lines 9-29); forming a cobalt film (116) and a buffer layer (120) on the whole structure (col. 4, lines 30-65); forming a cobalt mono-silicide film (normally depicted as (Co_xSi_y)) on the gate and the junction area, by performing a first RTP process (col. 4, lines 30-40); making a surface of the cobalt mono-silicide film amorphous to form an amorphous cobalt silicide film (col. 4, lines 30-40); and forming a cobalt di-silicide ($CoSi_2$), by removing the non-reacting cobalt film (col. 4, lines 30-40) and then performing a second RTP process (col. 4, line 67-col. 5 line 23) (claim 1). Kwon shows the method substantially as claimed in Figs. 3A-5 and corresponding text as: forming a gate (109) on a predetermined area of a semiconductor substrate (100) (col. 3, line 56-col. 4, line 8), forming spacers (110a, 112a) on sidewalls thereof (col. 4, lines 9-29), and then forming a junction area (114) in a predetermined area of the semiconductor substrate (col. 4, lines 9-29); forming an insulating film (110, 112) on the whole structure and then removing the insulating film on an area in which a silicide film should be formed (Figs. 3A-3B) (col. 3, line 56-col. 4 line

29); making the cobalt film (116) react with the gate and the junction area from which the insulating film is removed and exposed, to form a cobalt mono-silicide film, by performing a first RTP process (col. 4, lines 30-40); making a surface of the cobalt mono-silicide film amorphous to form an amorphous cobalt silicide film (col. 4, lines 30-40); and forming a cobalt di-silicide film by removing the non-reacting cobalt film (col. 4, lines 30-40) and then performing a second RTP process (col. 4, line 67-col. 5 line 23) (claim 8).

Kwon lacks anticipation in not explicitly teaching the steps of: 1) making a surface of the cobalt mono-silicide film amorphous to form an amorphous cobalt silicide, by performing a carbon ion implanting process; and forming a cobalt di-silicide film, by removing the non-reacting cobalt film and the buffer layer and then performing a second RTP process (claim 1); 2) forming the buffer layer of TiN film (claim 3); and 3) making a surface of the cobalt mono-silicide film amorphous to form an amorphous cobalt silicide, by performing a carbon ion implanting process; and forming a cobalt di-silicide film, by removing the non-reacting cobalt film and the TiN film and then performing a second RTP process (claim 8).

Dass teaches the formation of a cobalt silicide layer. In fig. 4 Dass shows a cobalt silicide layer (13) formed on a silicon substrate (10) with TiN film (placed on top of the cobalt silicide layer (col. 4, lines 28-43). Then the TiN layer is chemically removed from the top of the cobalt silicide (col. 4, lines 44-57). In figure 6 an ion implantation step is carried out which lead to an amorphized cobalt silicide layer. Any ion (such as carbon) able to cause the growth of an amorphous cobalt silicide layer can

be used, during the ion implantation of the cobalt silicide (col. 4, line 58-col. 5, line 8). Then the substrate undergoes a second RTP process carried out with inert gases in a nitrogen ambient. The cobalt atoms aid in the formation of shallow junctions do to the fact that cobalt does not form tightly bonded compounds with boron or arsenic two widely used dopant ions (col. 1, lines 56-65). Additionally, the process helps to reduce source/drain resistance.

Mikagi deals with the formation of a cobalt silicide layer. In the discussion of how to form a low resistance cobalt silicide it is discussed how the implantation of carbon inhibits the proper growth of the low resistance cobalt silicide layer and cause the layer to take on amorphous characteristics (col. 2, lines 20-49).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in Kwon by forming the amorphous cobalt by implanting carbon, and forming the cobalt di-silicide layer by removing a buffer layer made of TiN and then introducing the substrate to a RTP process as taught by Dass and the teachings of Mikagi with the motivation that Dass forms a cobalt silicide layer that aids in the formation of shallow junctions do to the fact that cobalt doesn't form tight bonded compounds with boron and arsenic and also reduces source/drain resistance.

Response to Arguments

5. Applicant's arguments filed 4/21/2005 in Application No. 10/731481 have been fully considered but they are not persuasive. The buffer layer and Co are removed in (col. 4, lines 30-40). In response to applicant's argument that there is no suggestion to

combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, all of the prior art in question deal with cobalt silicide formation.

Allowable Subject Matter

6. Claims 2,4, and 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 9-19 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...the first RTP process is performed at a temperature of 430°C to 530°C for a time of 10 to 60 seconds, by introducing nitrogen gas, argon gas, helium gas and hydrogen gas at a flow rate of 10 to 1000 sccm, respectively, as required by claim 5;

...the carbon ion implanting process is performed up to a depth of 50Å to 1000Å with an energy of 10 to 100 keV and a dose of $1x10^{14}$ to $1x10^{16}$ atoms/cm^2, as required by claim 6;

... the second RTP process is performed at a temperature of 650°C to 800°C for a time of 5 to 30 seconds, by introducing nitrogen gas, argon gas, helium gas and hydrogen gas at a flow rate of 10 to 1000 sccm, respectively, as required by claim 7; and

...wherein the carbon ion implanting process is performed up to a depth of 50Å to 1000Å with an energy of 10 to 100 keV and a dose of $1x10^{14}$ to $1x10^{16}$ atoms/cm^2, as required by claims 9 and 15.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WLL
May 5, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER